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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/828,083	04/05/2001	James O. Barnes	10010738-1	5481

7590 10/17/2003

AGILENT TECHNOLOGIES
Legal Department, 51U-PD
Intellectual Property Administration
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EXAMINER	
LE, DON P	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/828,083	BARNES, JAMES O.	
	Examiner	Art Unit	
	Don P Le	2819	

-- Th MAILING DATE of this communication app ars on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,5,6,11 and 12* is/are allowed.

6)☐ Claim(s) *1, 2, 4, 7-10, 13-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(B) as being anticipated by Gould et al. (US 5,051,917).

3. With respect to claim 1, figure 6 of Gould discloses an integrated circuit comprising:

Functional circuit blocks (22, 58) that are spaced apart from one another, each block having a respective boundary that surrounds the block (there is a boundary surround the block);

A region (54, 56) disposed outside the boundary of the functional circuit blocks and devoid of functional circuitry blocks; and

A transistor (one of the transistors in 54) disposed in the region.

4. With respect to claim 2, figure 6 of Gould discloses the functional circuit block is configured to perform a predetermined function (standard cell is designed to perform a logic function).

5. With respect to claim 4, figure 6 of Gould discloses the transistor is a FET (transistor in 54).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7-10 and 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gould et al. (US 5,051,917). Figure 6 of Gould discloses an integrated circuit, comprising:

Functional circuit blocks that are spaced apart from one another (22, 58); and

A region devoid of the functional circuitry (54);

The apparatus of Gould does not specifically show a buffer or logic circuit disposed in the region. However, Gould teaches that the gate array 54 can be connected to form a buffer as a matter of design choice for the purpose of connecting with other logic circuit to form a more complex circuit. It would have been obvious to one of ordinary skill of art at the time the invention was made to have implemented the apparatus of Gould having the gate array forming a buffer for the purpose of connecting with other logic circuits to form a more complex logic circuit.

8. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gould et al. (US 5,051,917) in view of Patel et al. (US 6,414,518). Figure 6 of Gould discloses an integrated circuit, comprising:

A conductive path (inherent that there is a conductive path in a circuit);

Functional circuitry blocks (22, 58), each block having a respective boundary that surrounds the block (there is a boundary surround the block);

A region devoid of the functional circuitry (54),; and

A transistor (transistor in 54) disposed in the region.

The apparatus of Gould does not show the transistor connected as claimed. Figure 10C of Patel discloses a spare transistor (1060, or 1064) having a pair of terminals connected to a conductive path and having a control terminal for the purpose to be used in a logic circuit. It would have been obvious to one of ordinary skill of art at the time the invention was made to have implemented the apparatus of Gould having a transistor connected as shown by Patel for the purpose of having a spare transistor.

Allowable Subject Matter

9. Claims 3, 5, 6, 11 and 12 are allowed.

10. The following is an examiner's statement of reasons for allowance:

With respect to claim 3, the prior art does not teach one of the functional circuit blocks is unconfigurable.

With respect to claims 5 and 6, the prior art does not teach placed of transistor after the functional blocks are placed.

With respect to claims 11 and 12, reasons for allowance were given in previous Office Action dated 12/18/02.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

11. Applicant's arguments filed 8/28/03 have been fully considered but they are not persuasive.

12. With respect to claims 1, 7, 8, 13, 17, 20 and 21, the addition of new limitations (boundary surrounds the blocks) is still anticipated in that there are boundaries surround the blocks as shown by Gould.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P Le whose telephone number is 703-308-4890. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

October 14, 2003

DON LE
PRIMARY EXAMINER